دانشگاه صنعتی امیرکبیر

دانشکده مهندسی برق

طراحی مدارهای VLSI

فصل هفتم: مدار های ترتیبی

بخش اول : مدار های ترتیبی ایستا

مجید شالچیان

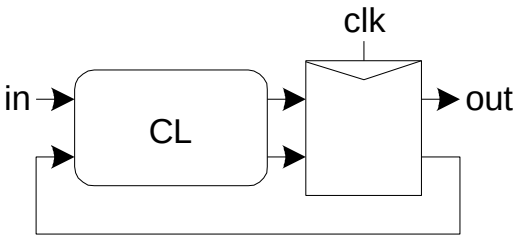
مقدمه

خروجی تابع ورودی و state فعلی مدار است.

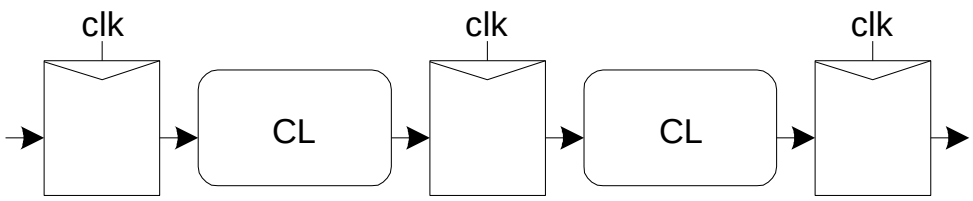
نیاز به جداسازی حالت قبلی و حالت فعلی و رعایت ترتیب حالت ها

پیاده سازی با مدار ترتیبی و رجیستر

مثال: Pipeline و FSM



Finite State Machine



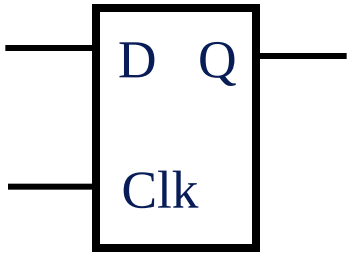
Pipeline

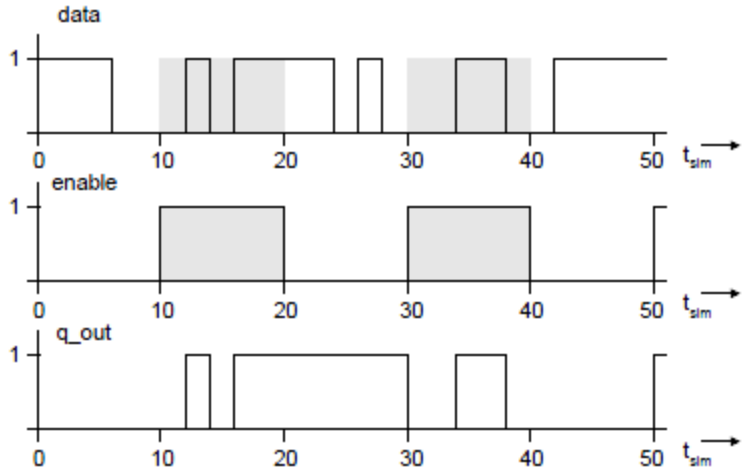
رجیستر های ایستا و پویا

- رجیستر های ایستا
  - حالت را تا زمانیکه منبع تغذیه روشن است نگهداری می کنند.
  - مبتنی بر وجود حلقه فیدبک مثبت بین خروجی و ورودی عمل می کنند.
  - وقتی تغییرات سیگنال چندان سریع نیست می توان با clock gating توان را کم کرد.
- رجیستر های پویا
  - حالت در خازنهای پارازیتی ذخیره می شود.
  - برای زمان های بسیار کوتاه (میلی ثانیه) حالت را ذخیره می کنند.
  - نیاز به بازسازی متناوب سیگنال دارند (Refresh)
  - معمولا ساده تر دارای سرعتبالاتر و مصرف توان کمتر هستند.

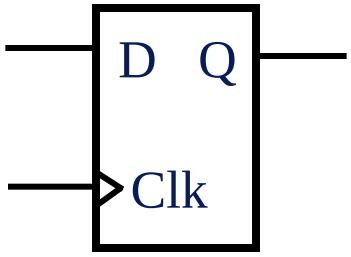
مقایسه Latch و Register

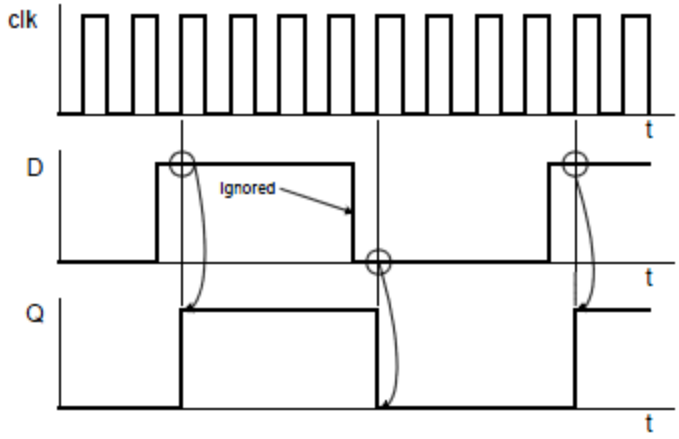
- Latch
  stores data when clock is low
  Transparent when clock is high





- Register (Edge Triggered) (ET)
  stores data when clock rises



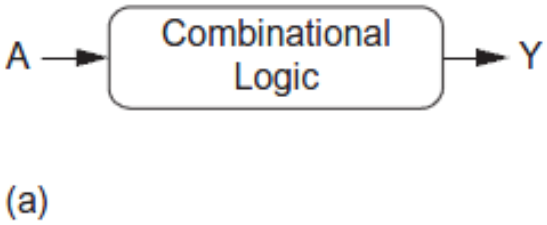


positive edge-triggered: $0 \rightarrow 1$
negative edge-triggered: $1 \rightarrow 0$

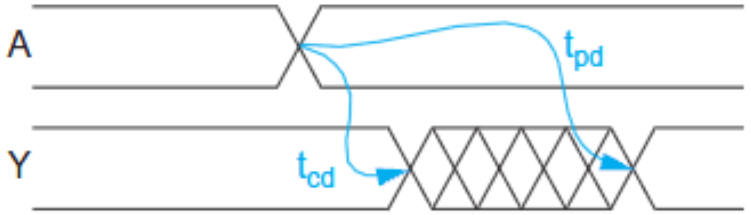
تاخیر ها

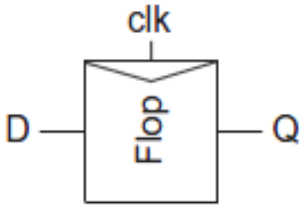
Term	Name
t_{pd}	Logic Propagation Delay
t_{cd}	Logic Contamination Delay
t_{pcq}	Latch/Flop Clock-to-Q Propagation Delay
t_{ccq}	Latch/Flop Clock-to-Q Contamination Delay
t_{pdq}	Latch D-to-Q Propagation Delay
t_{cdq}	Latch D-to-Q Contamination Delay
t_{setup}	Latch/Flop Setup Time
t_{hold}	Latch/Flop Hold Time

تعریف تاخیر ها

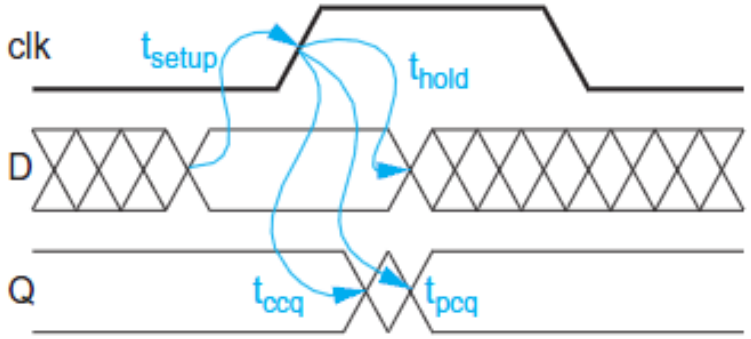


(a)

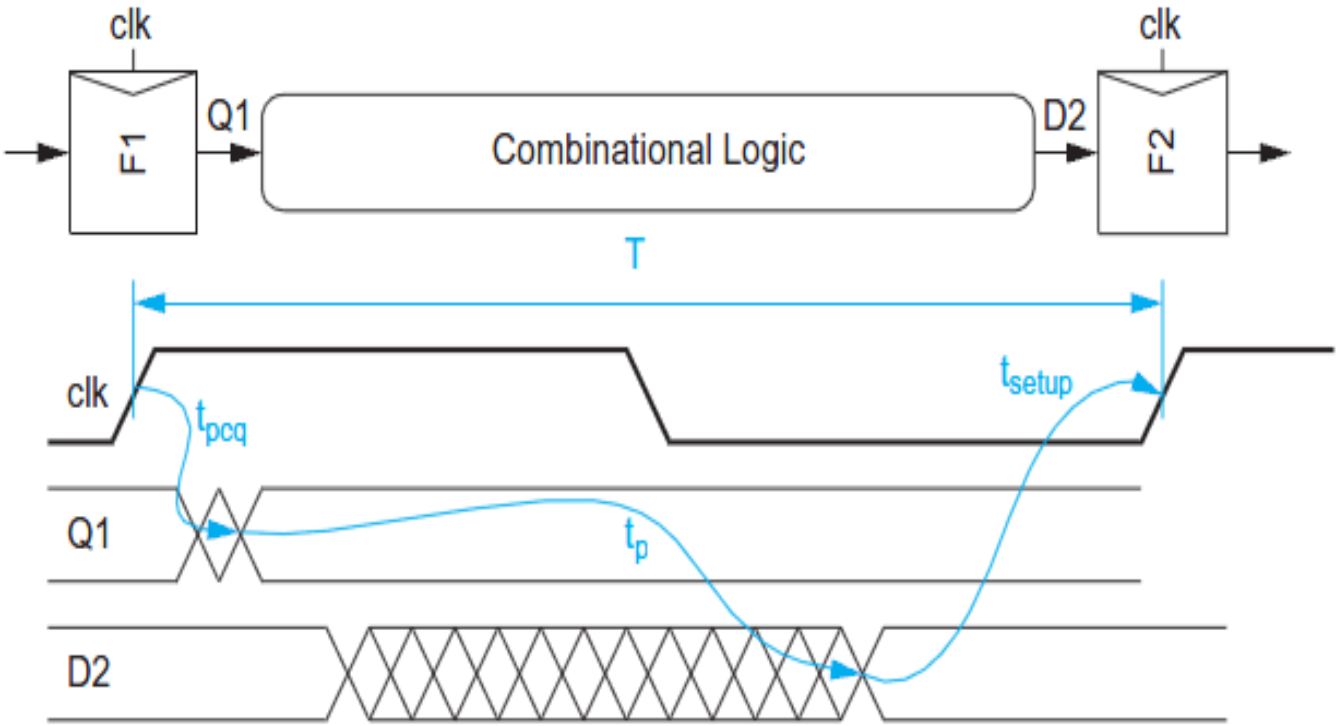




(b)

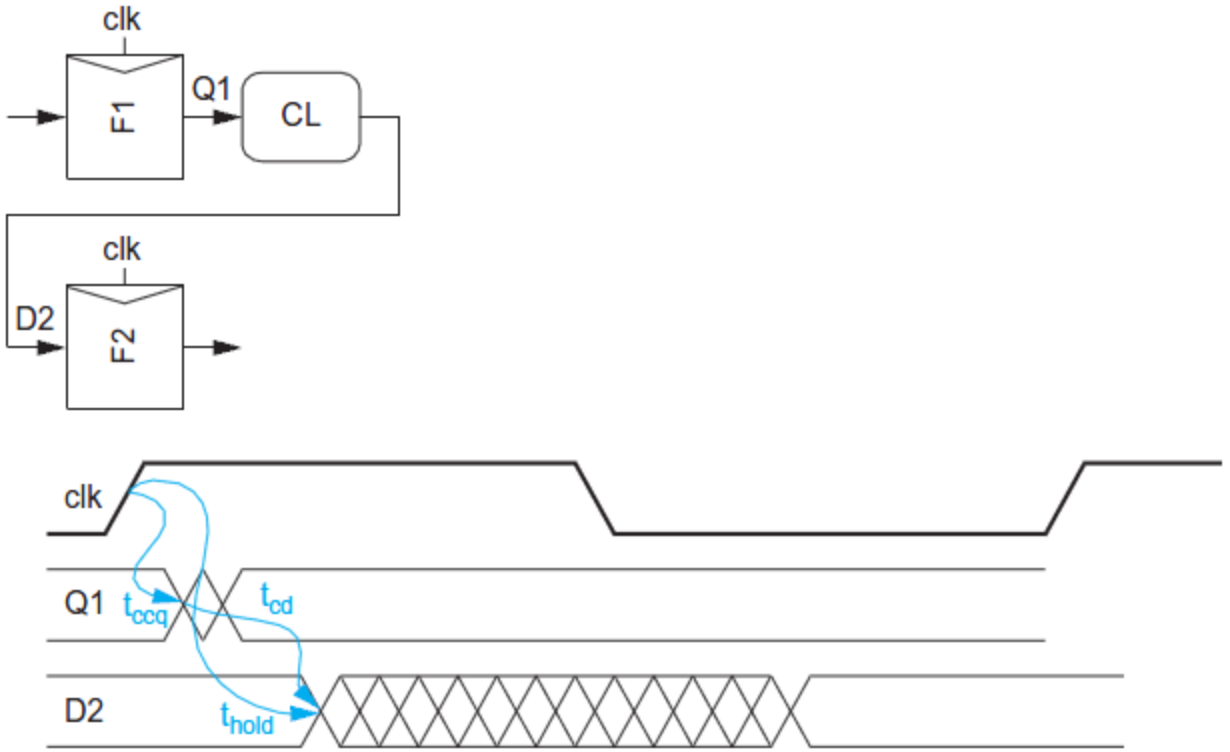


Maximum delay constraints



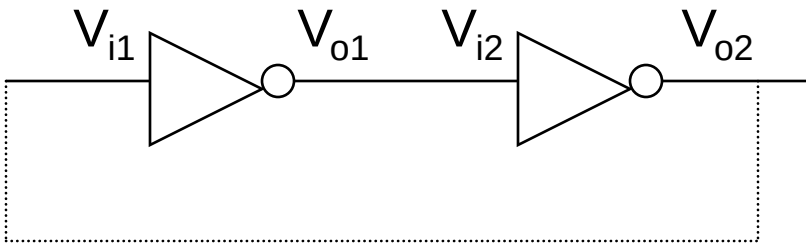
$$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$$

Minimum delay constraints

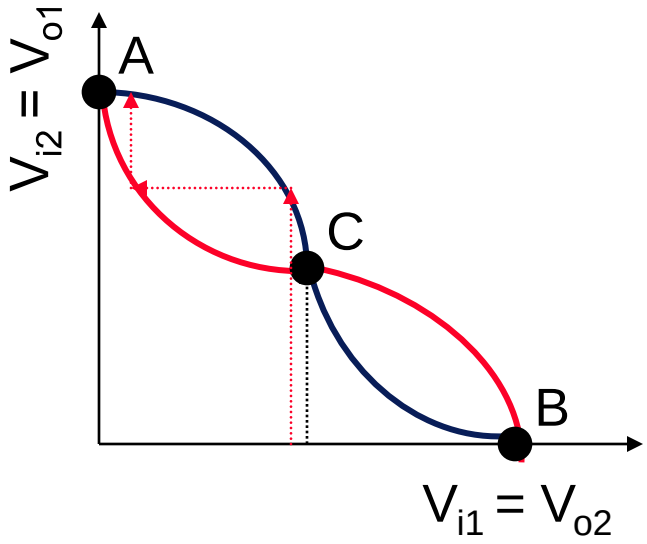


$$t_{ccq} + t_{cd} \geq t_{hold}$$

یادآوری خاصیت Regenerative



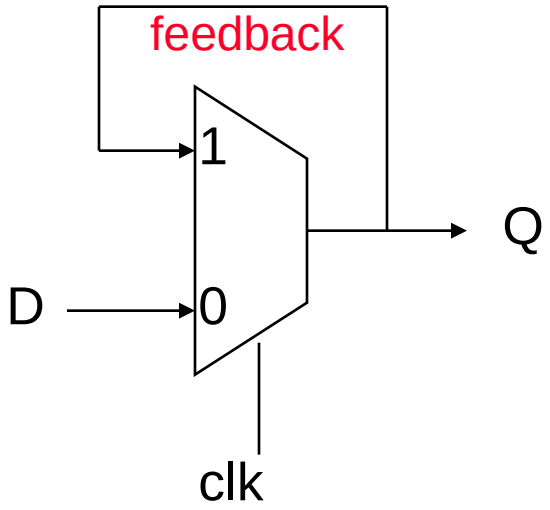
cascaded inverters



If the gain in the transient region is larger than 1, only A and B are stable operation points. C is a metastable operation point.

MUX Based Latches

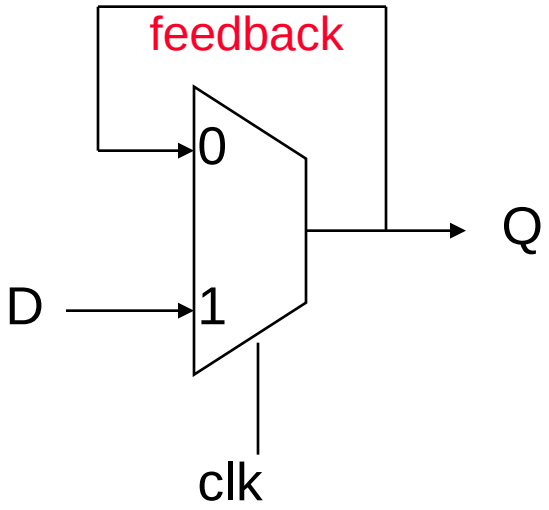
- Change the stored value by cutting the feedback loop



Negative Latch

Q = clk & Q | !clk & D

transparent when the clock is low

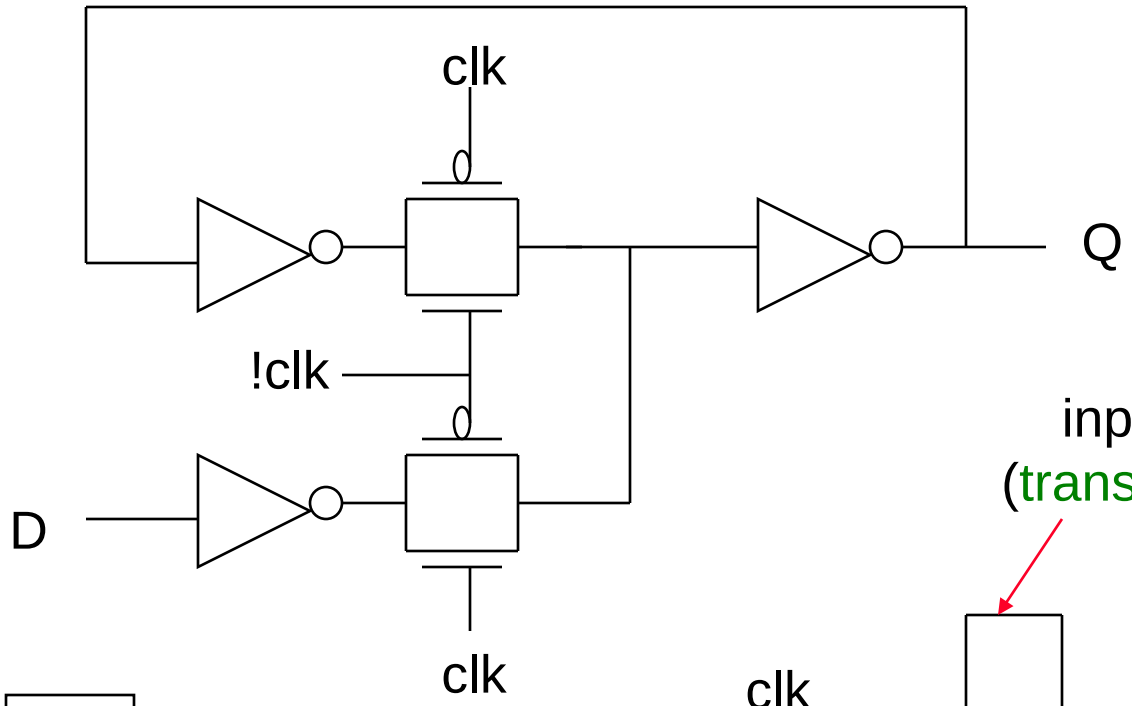


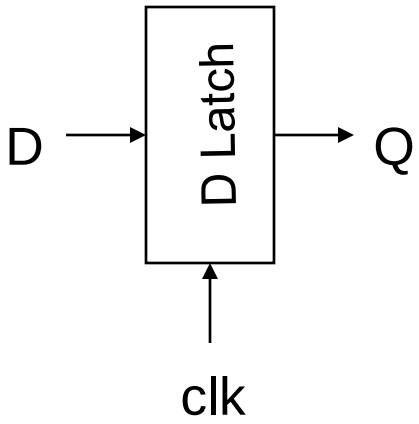
Positive Latch

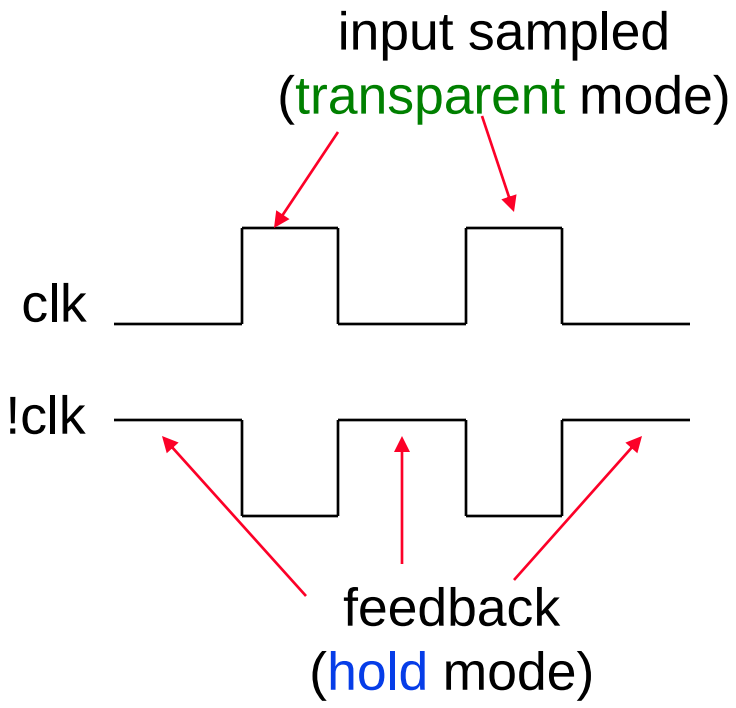
Q = !clk & Q | clk & D

transparent when the clock is high

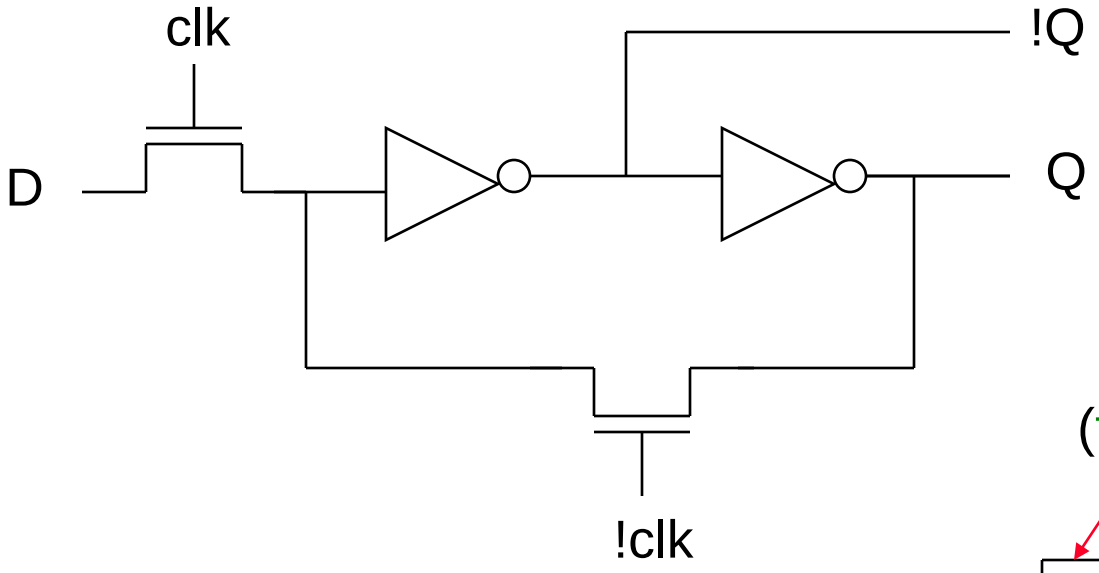
TG MUX Based Latch Implementation

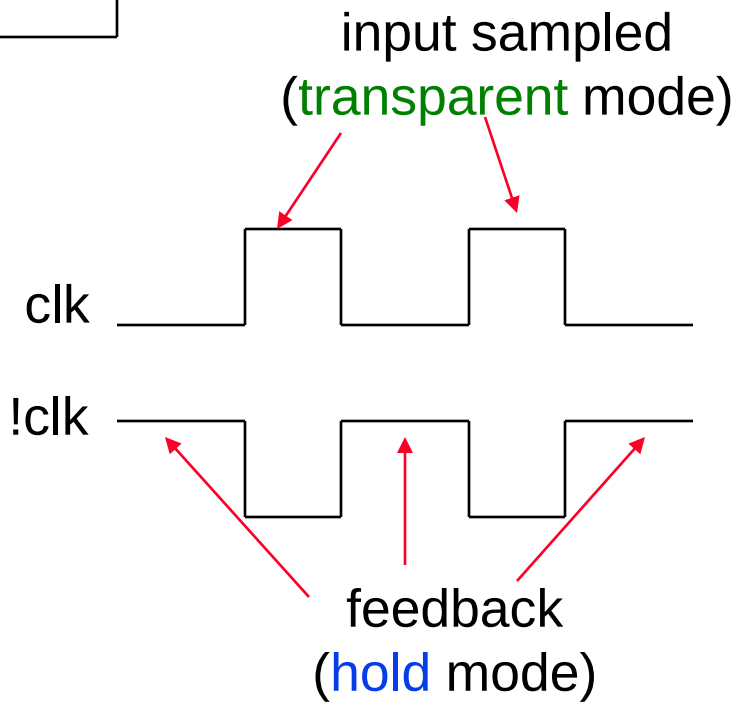






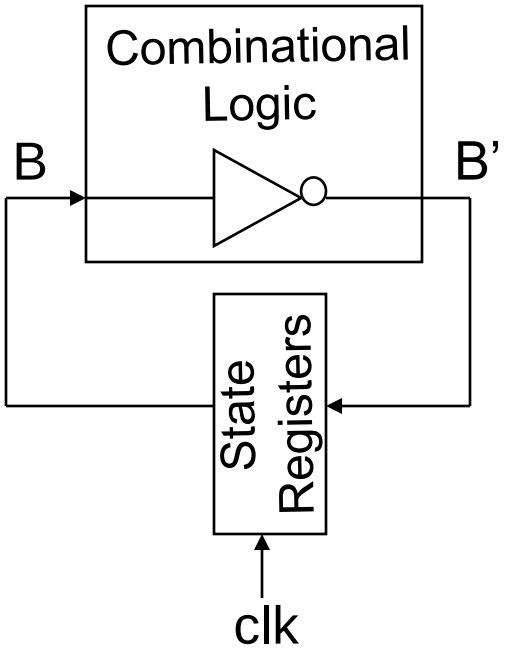
NMOS MUX Based Latch Implementation

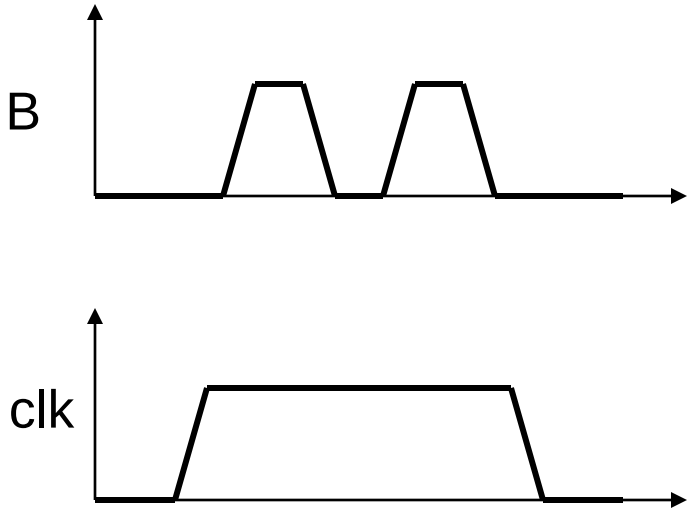




- Reduced clock load, but threshold drop at output of pass transistors so reduced noise margins and performance and power dissipation

Latch Race Problem





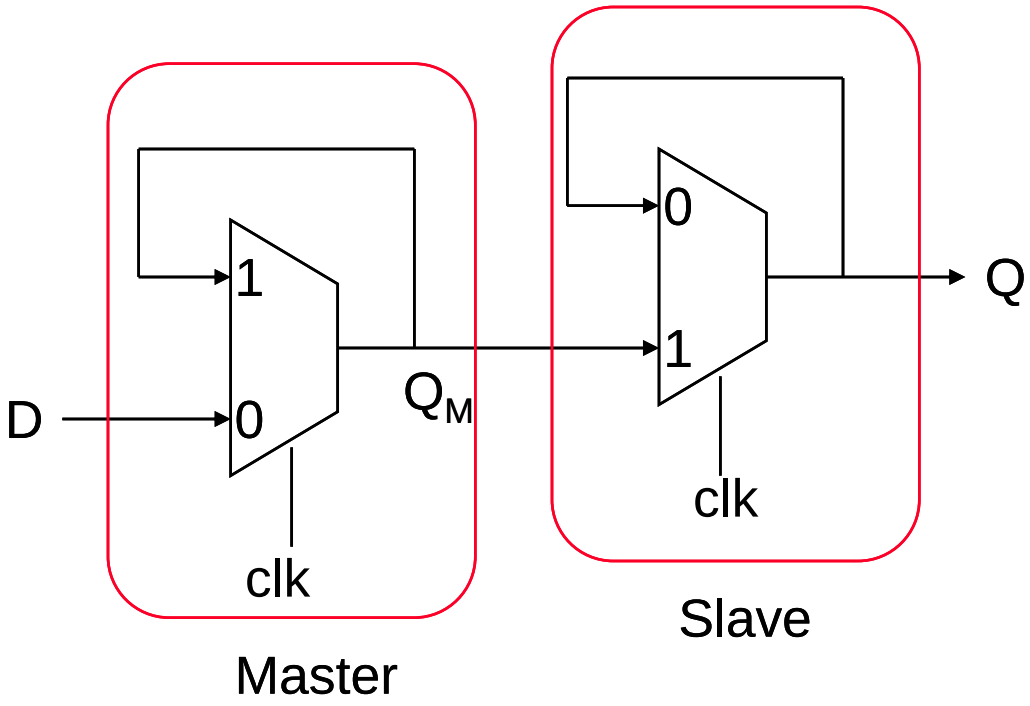
Which value of B is stored?

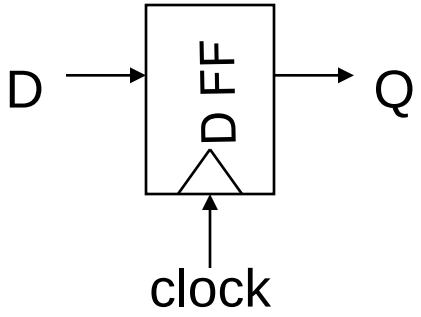
Two-sided clock constraint

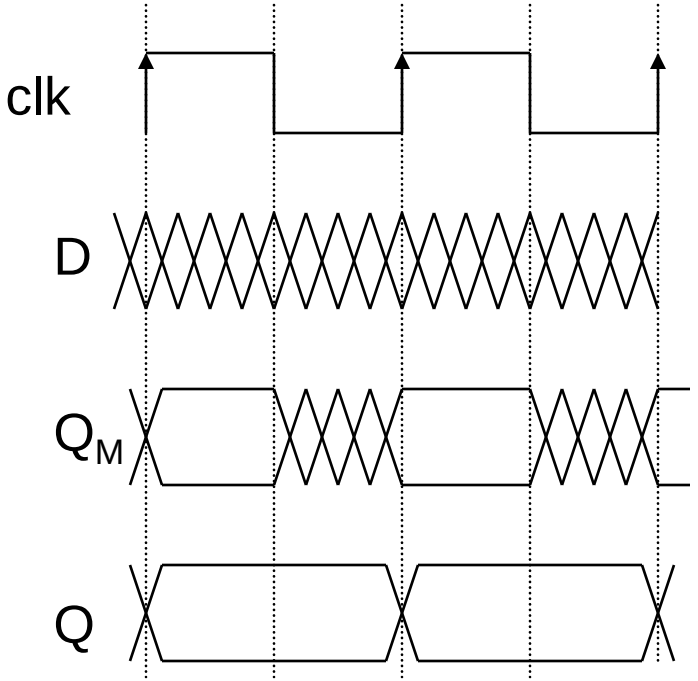
$$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$$

$$T_{high} < t_{c\text{-}q} + t_{cdlogic}$$

Master Slave Based ET Flipflop



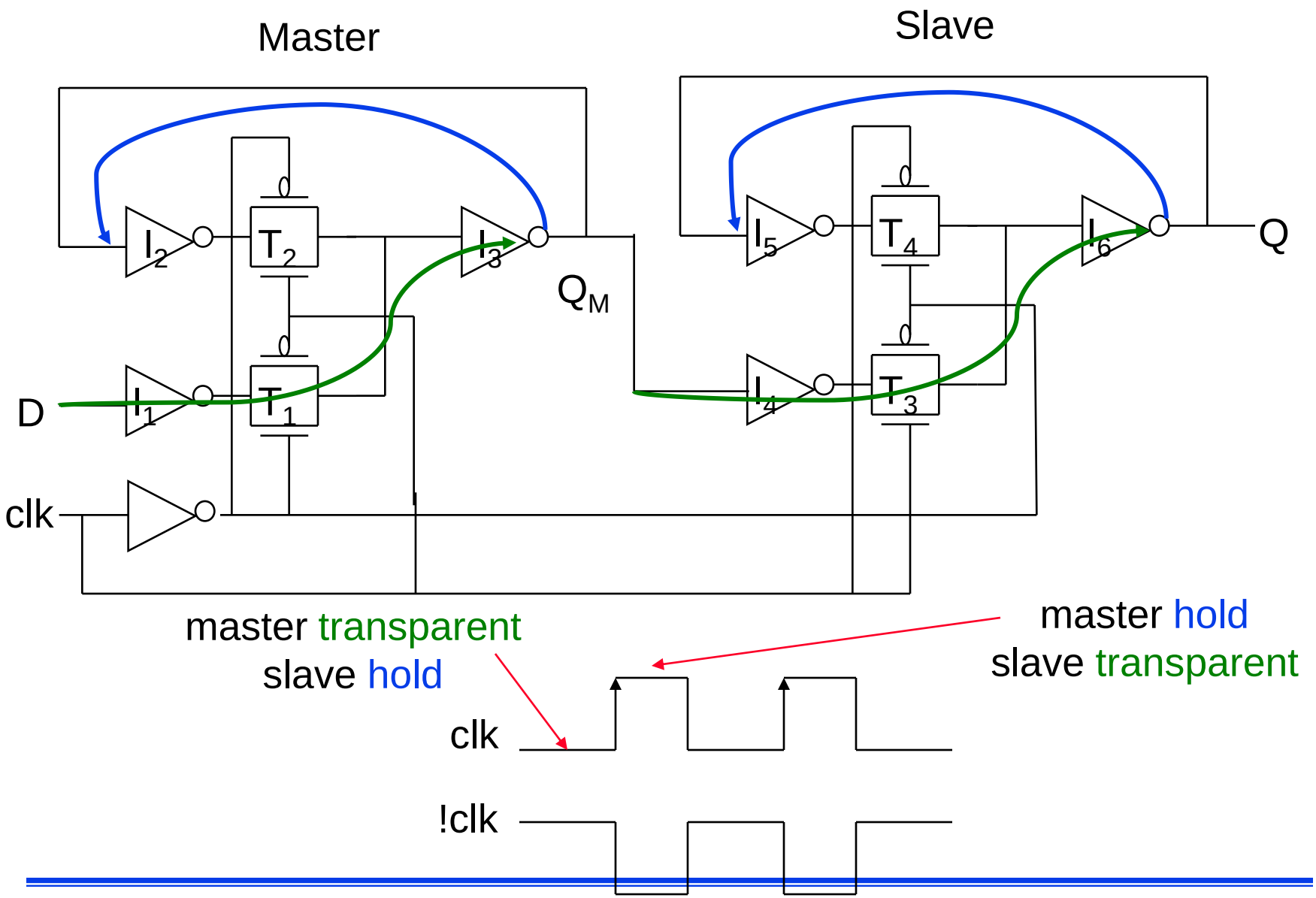




clk = 0 transparent hold

clk = 1 hold transparent

MS ET FF Implementation



MS Registr Timing Properties

- Assume propagation delays are t_{pd_inv} and t_{pd_tx}, that the contamination delay is 0, and that the inverter delay to derive !clk is 0
- Set-up time - time before rising edge of clk that D must be valid

$$3 * t_{pd\_inv} + t_{pd\_tx}$$

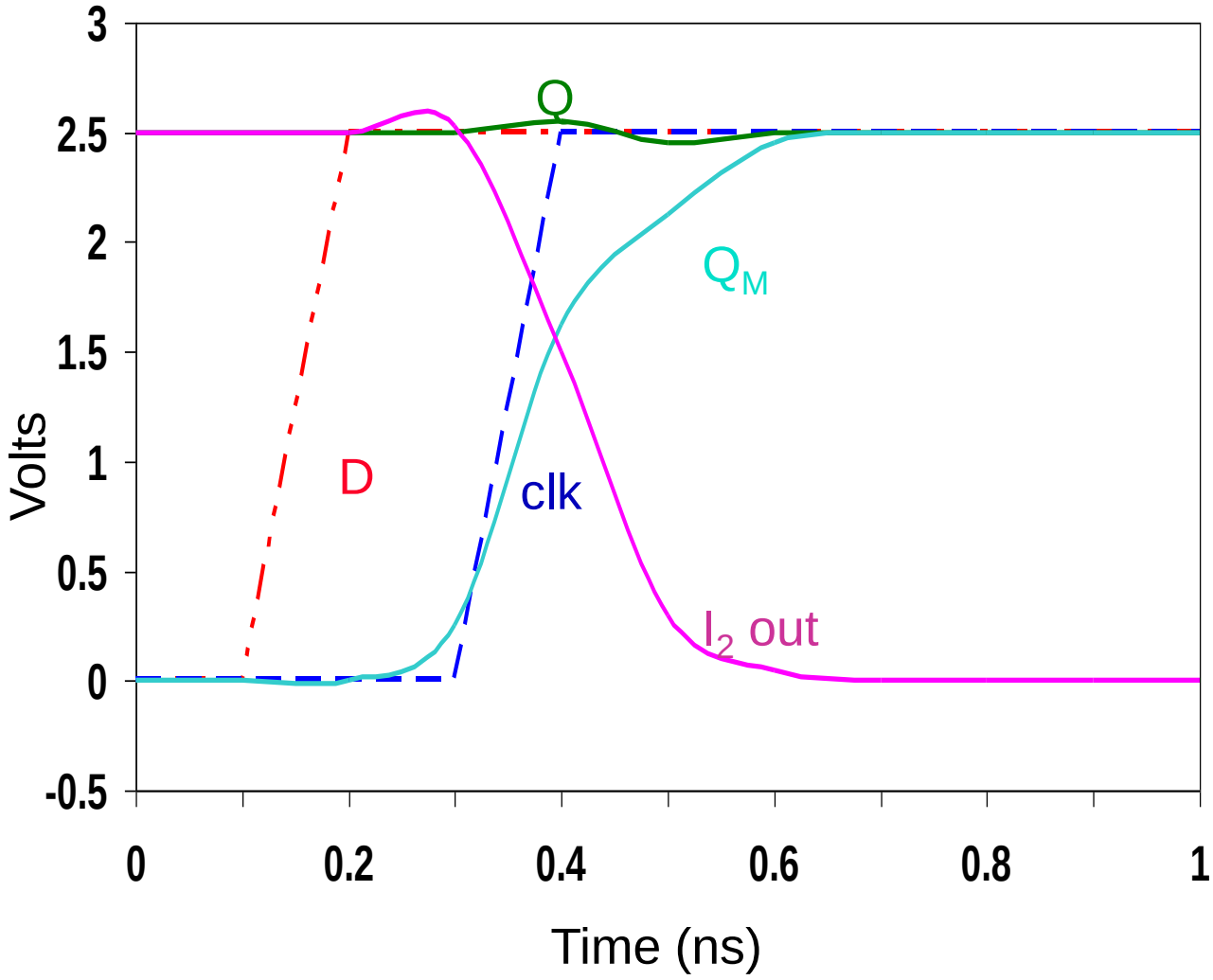
- Propagation delay - time for Q_M to reach Q

$$t_{pd\_inv} + t_{pd\_tx}$$

- Hold time - time D must be stable after rising edge of clk

zero

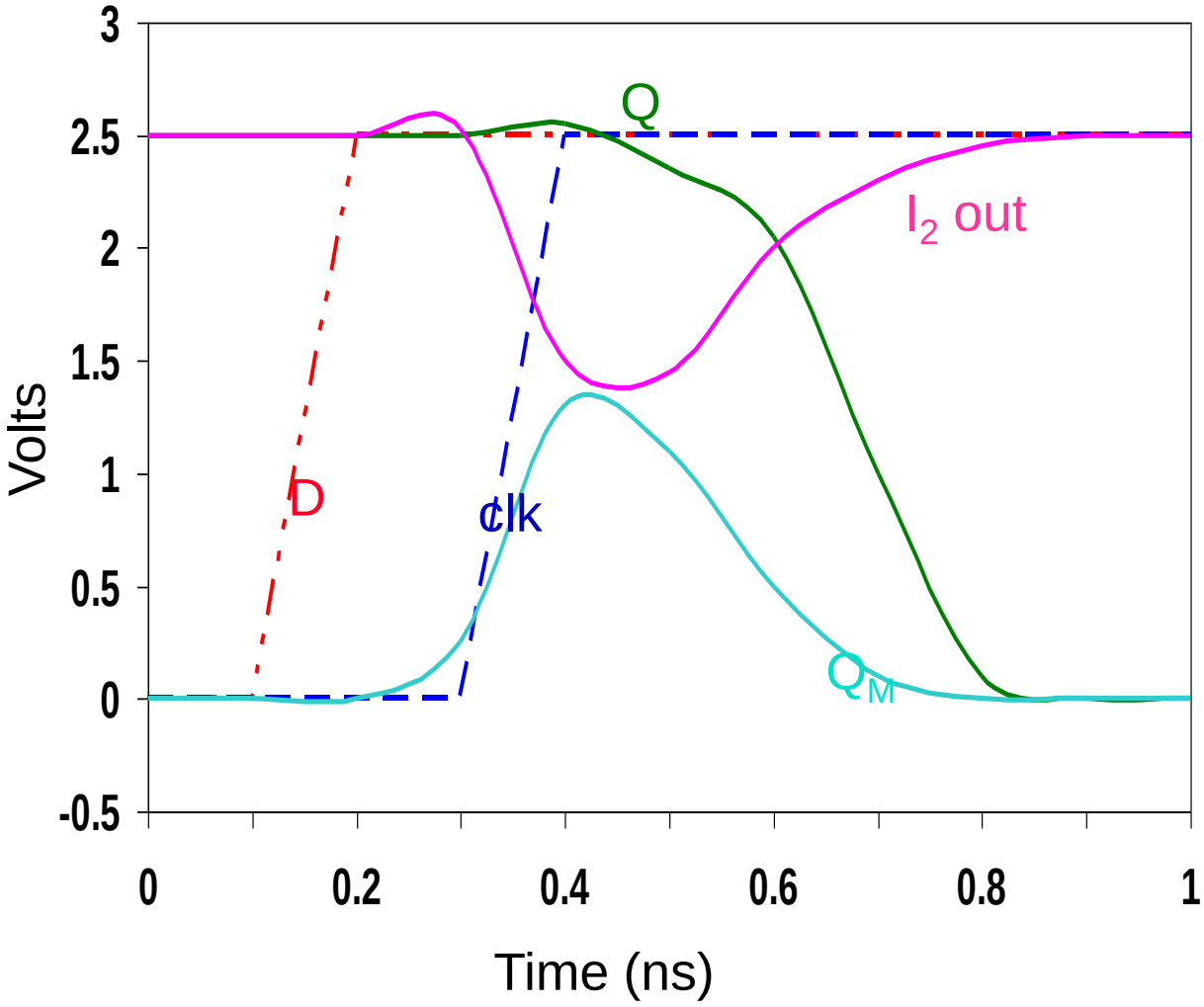
Set-up Time Simulation



t_{setup} = 0.21 ns

works correctly

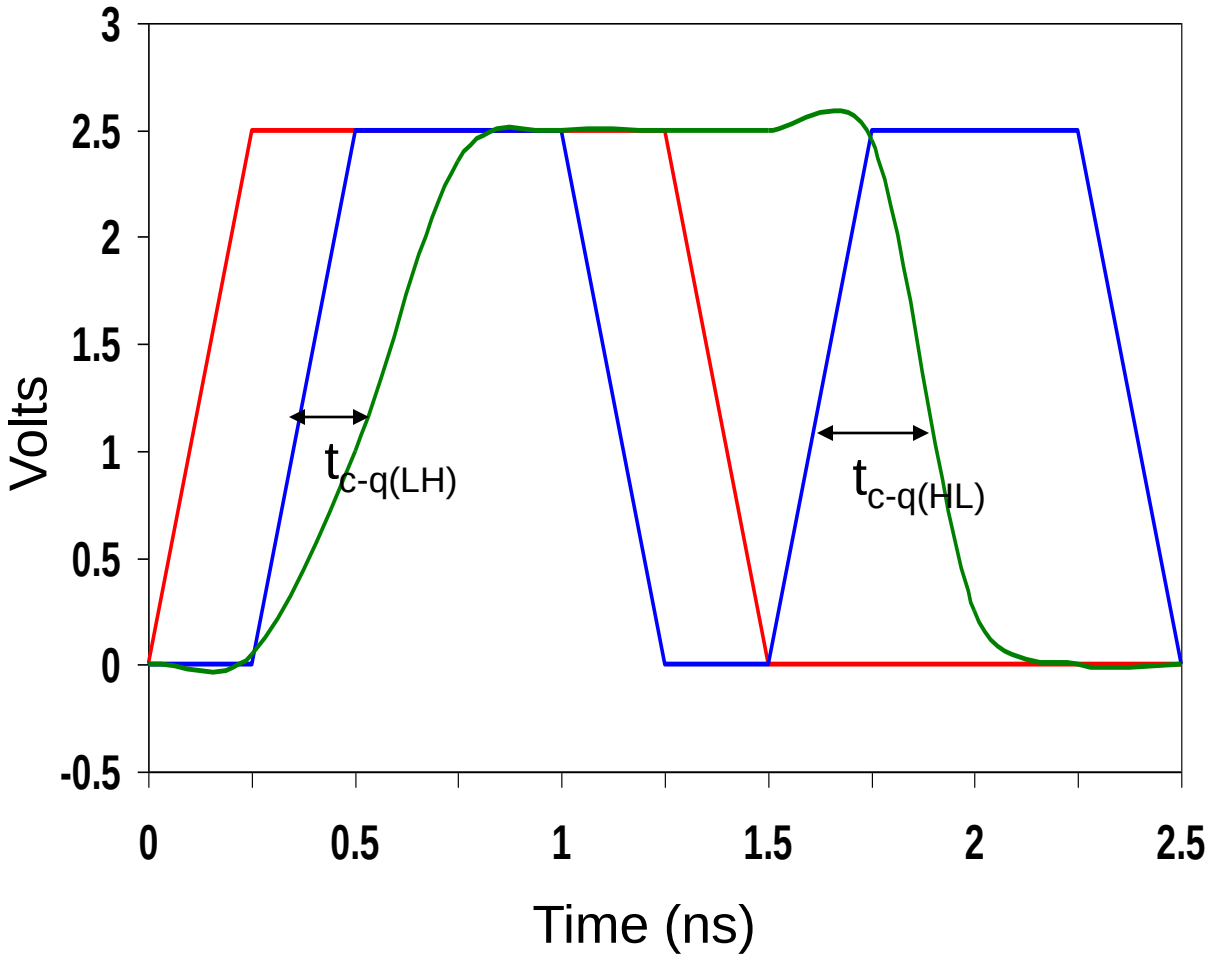
Set-up Time Simulation



t_{setup} = 0.20 ns

fails

Propagation Delay Simulation

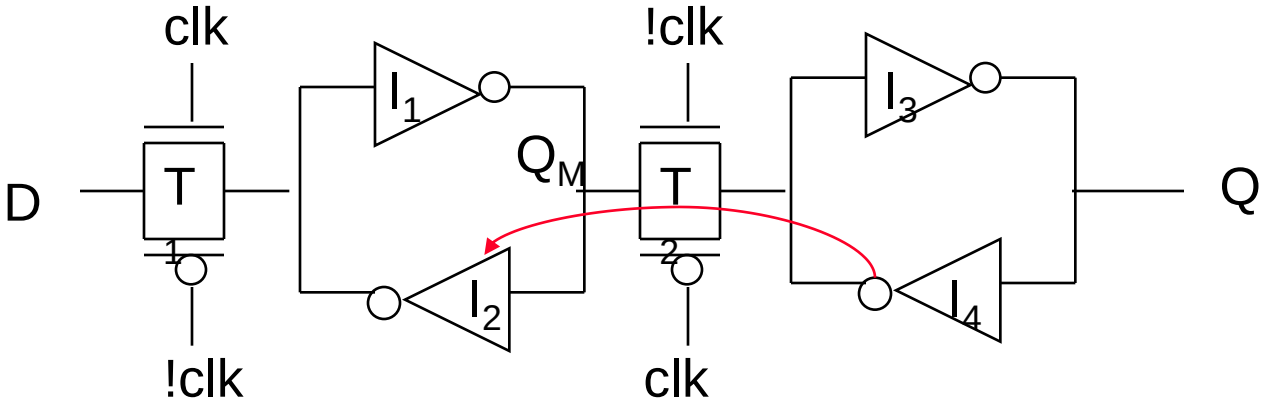


$t_{c\text{-}q(LH)}$ = 160 psec

$t_{c\text{-}q(HL)}$ = 180 psec

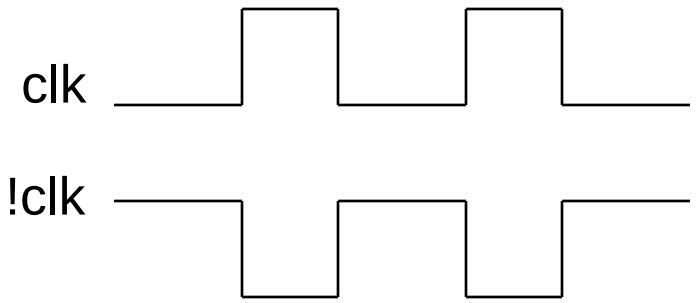
Reduced Load MS FF

- Clock load per register is important since it directly impacts the power dissipation of the clock network.
- Can reduce the clock load (at the cost of robustness) by making the circuit ratioed

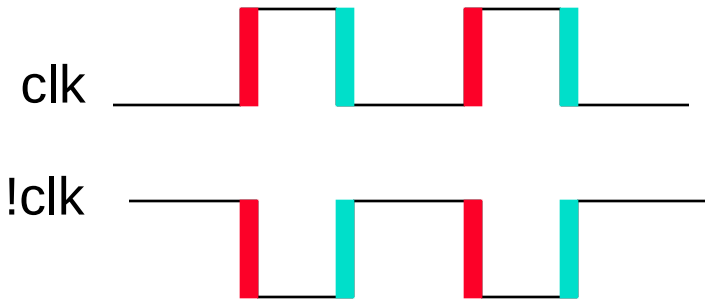


- to switch the state of the master, T_1 must be sized to overpower I_2
- to avoid reverse conduction, I_4 must be weaker than I_1

Non-Ideal Clocks



Ideal clocks



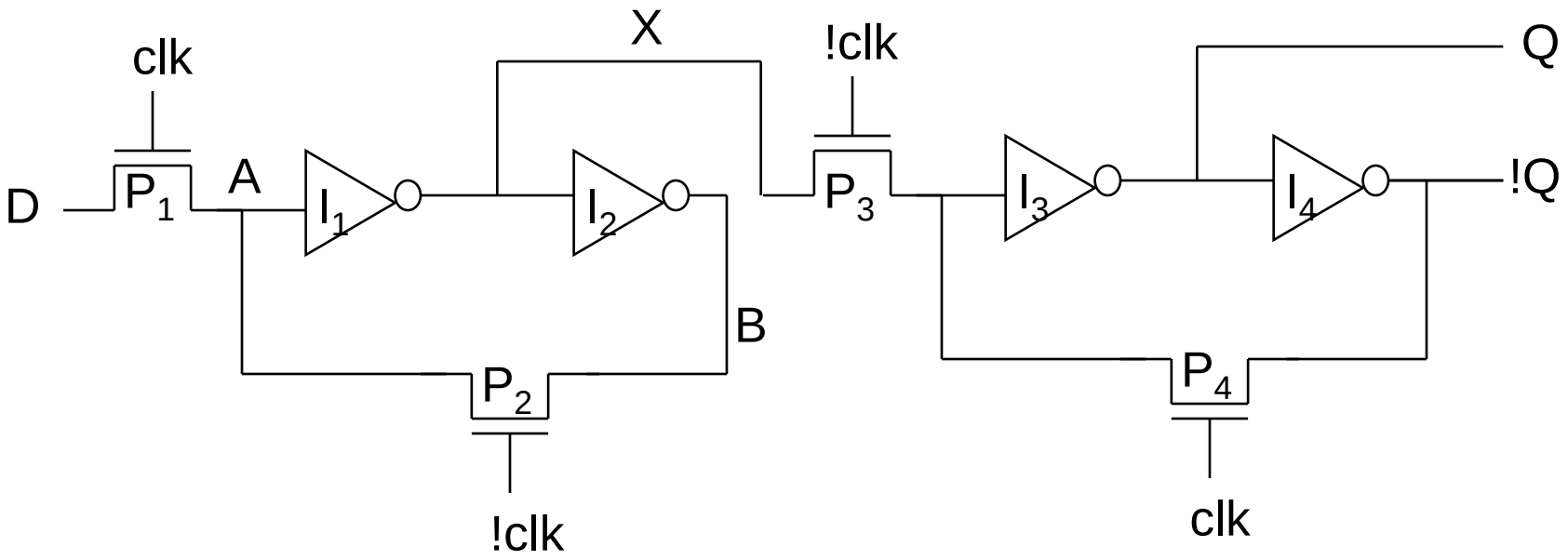
Non-ideal clocks

clock skew

1-1 overlap

0-0 overlap

Example of Clock Skew Problems

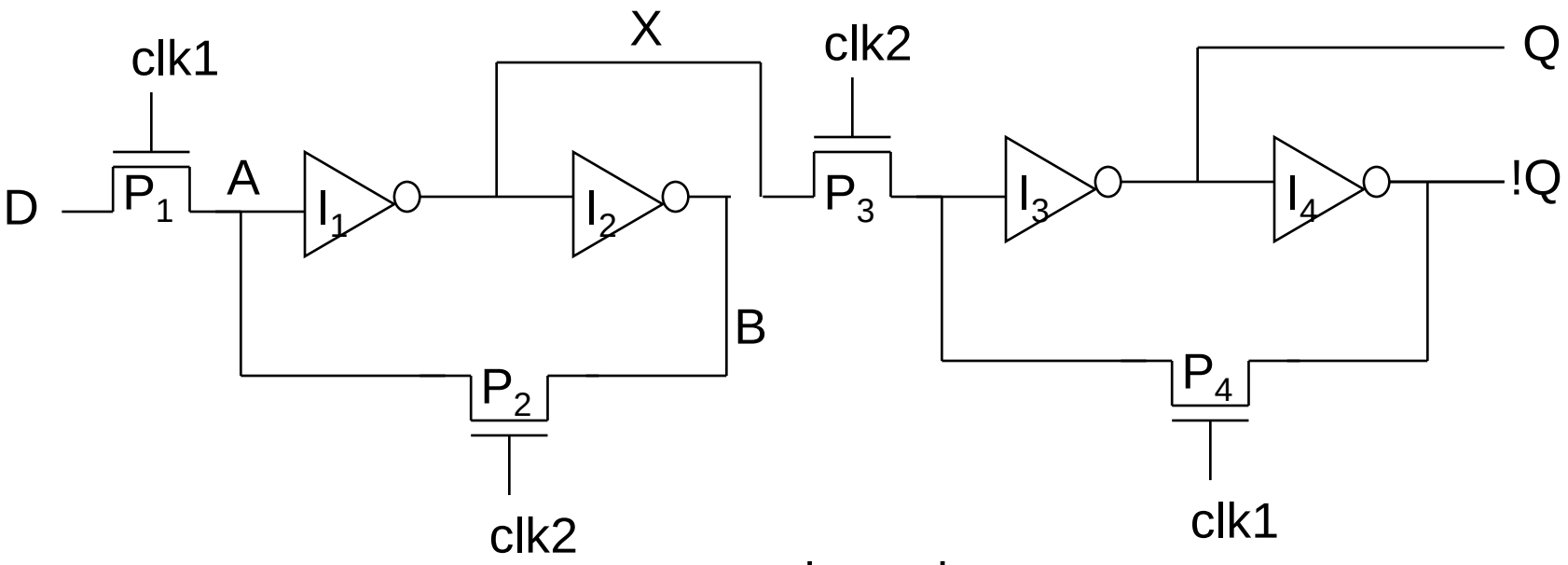


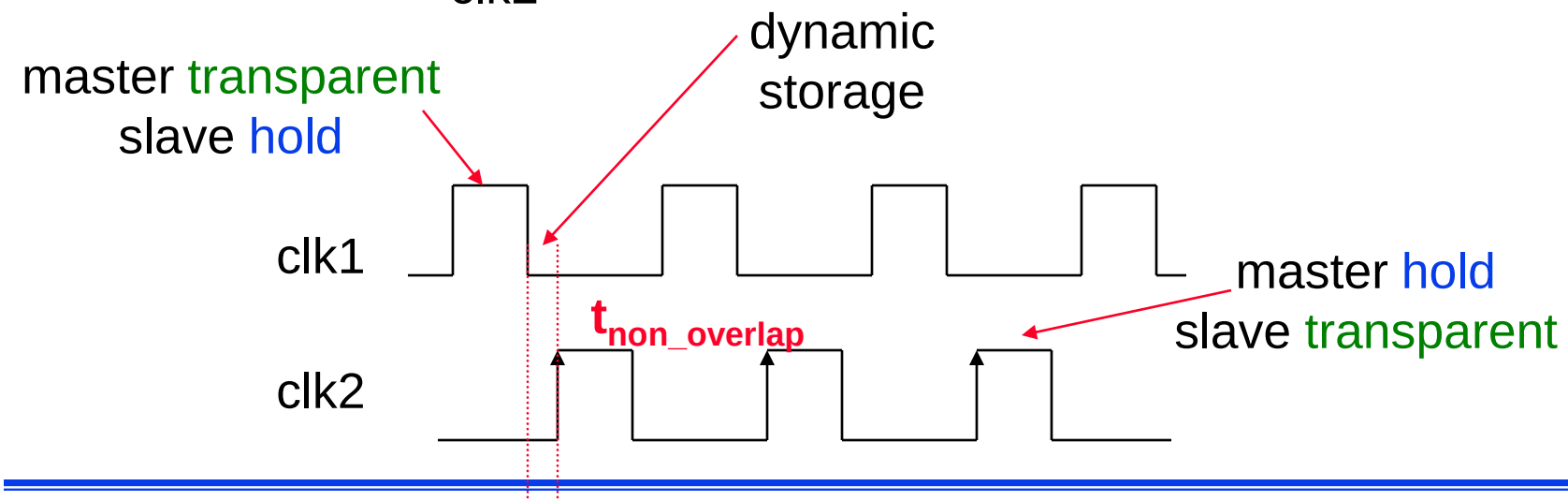
Race condition – direct path from D to Q during the short time when both clk and !clk are high (1-1 overlap)

Undefined state – both B and D are driving A when clk and !clk are both high

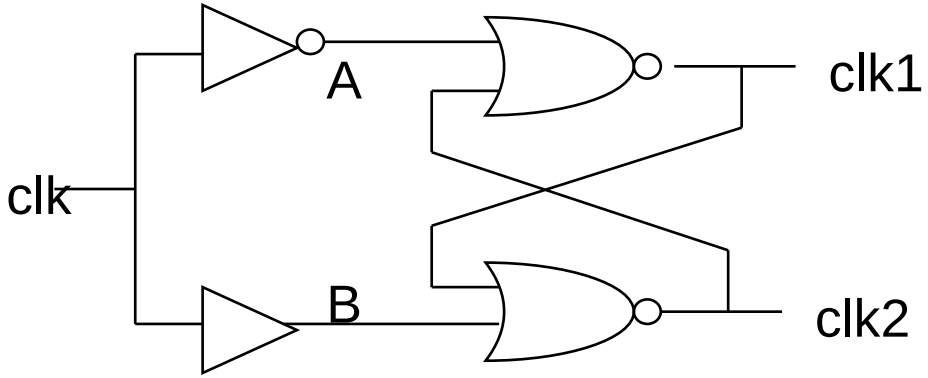
Dynamic storage – when clk and !clk are both low (0-0 overlap)

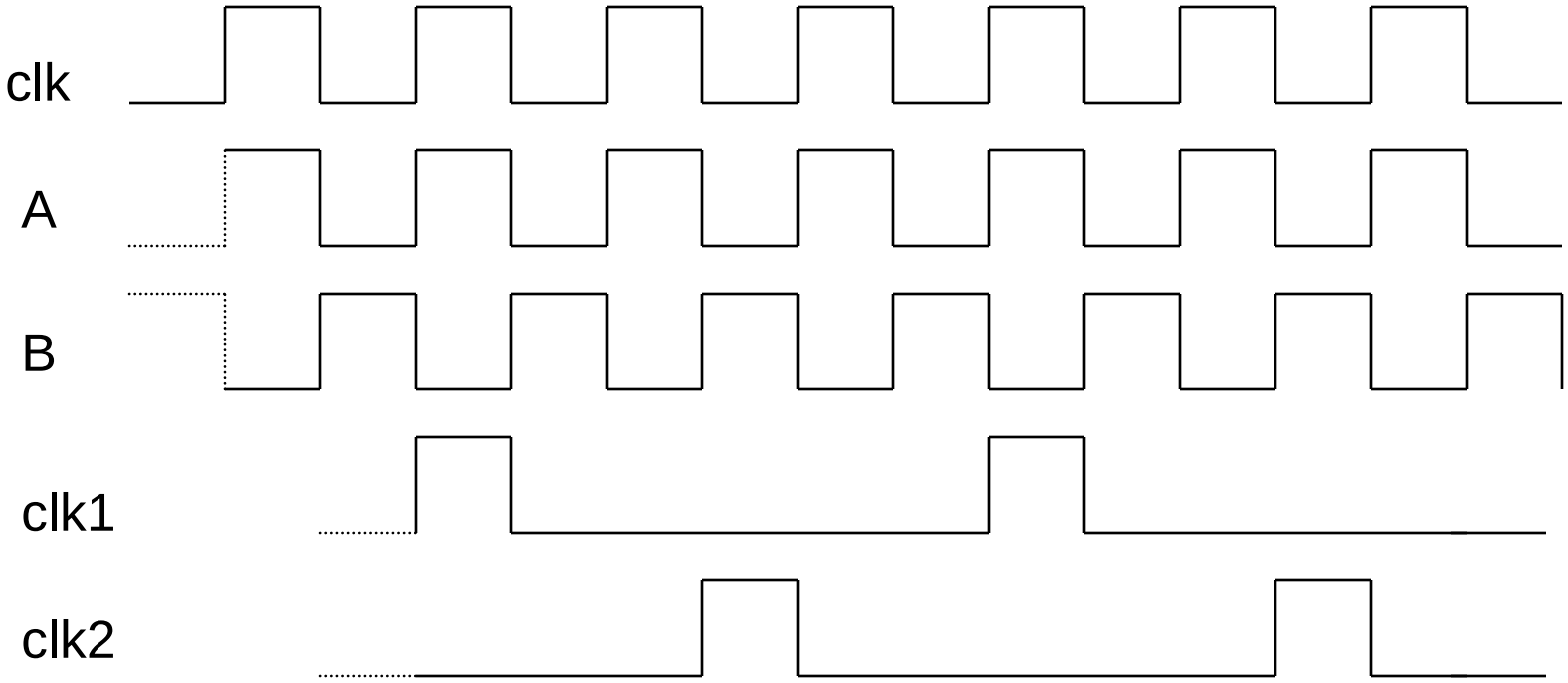
Pseudostatic Two-Phase ET FF



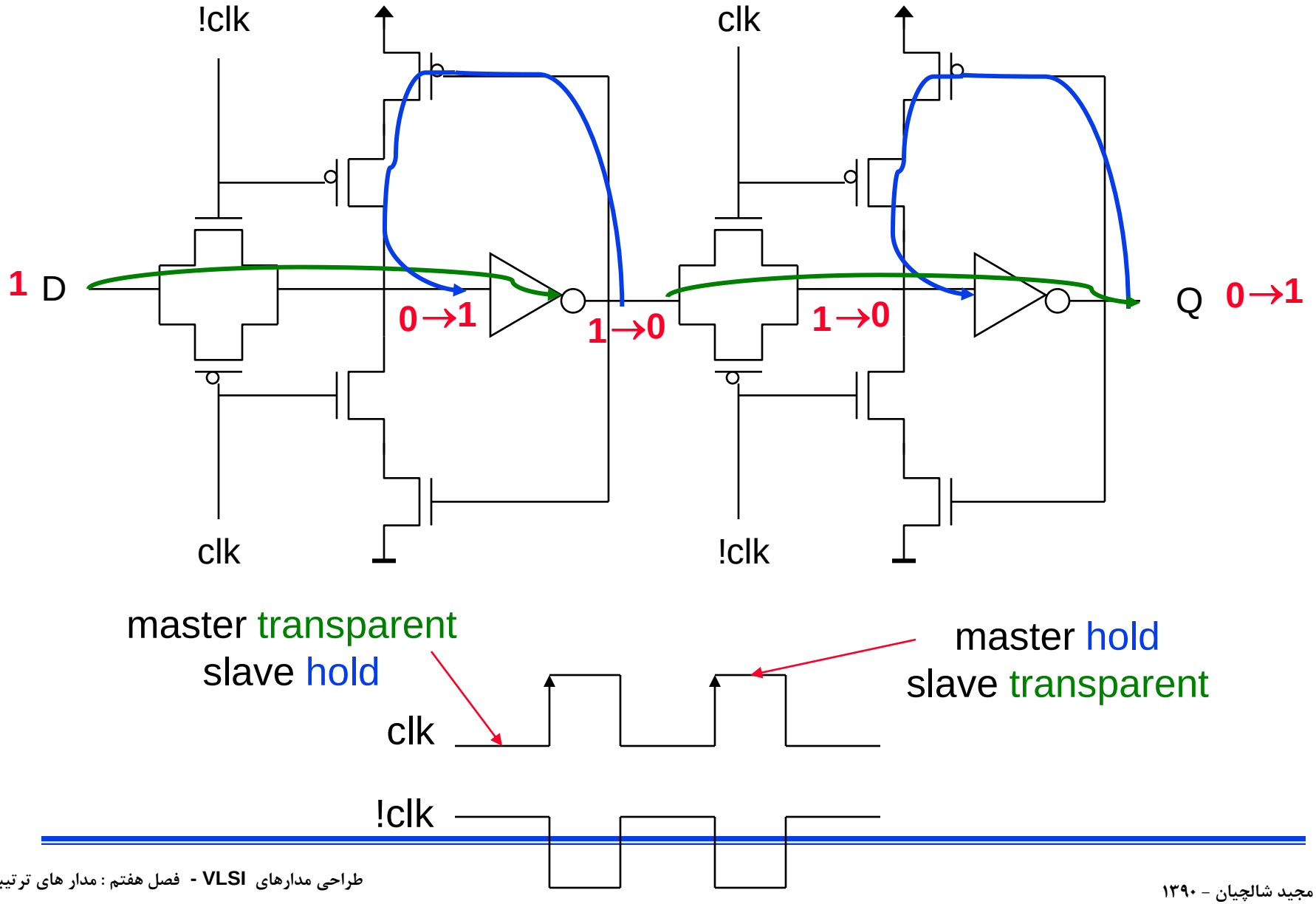


Two Phase Clock Generator



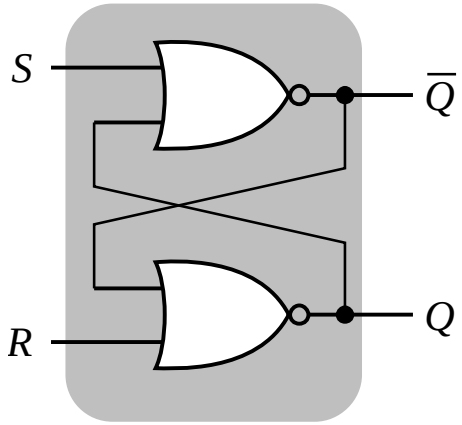


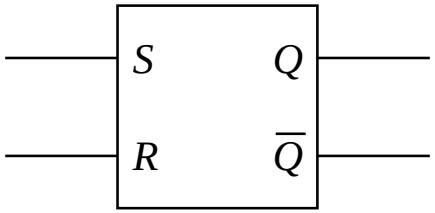
Power PC Flipflop



ساختار SR Latch

NOR-based set-reset



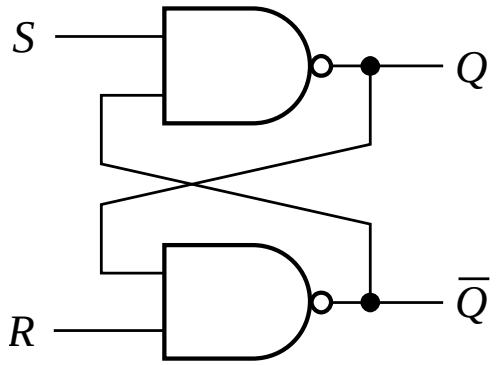


S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

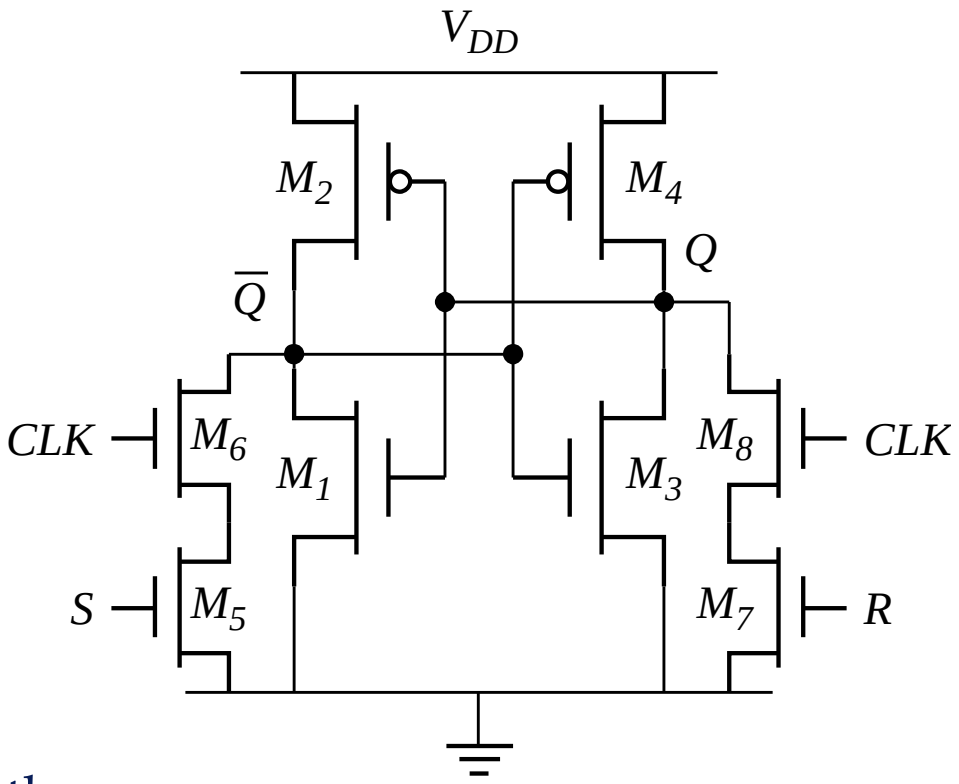
Forbidden State

Cross-Coupled NAND

Cross-coupled NANDs

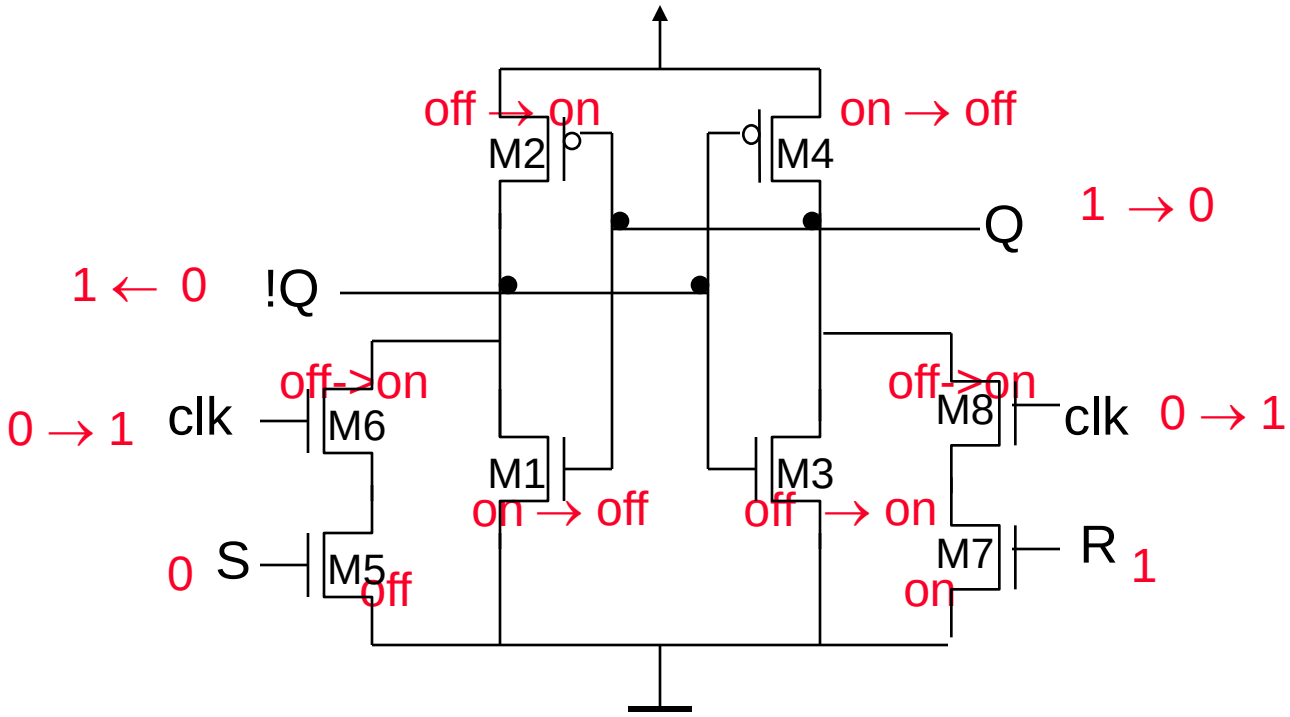


Added clock

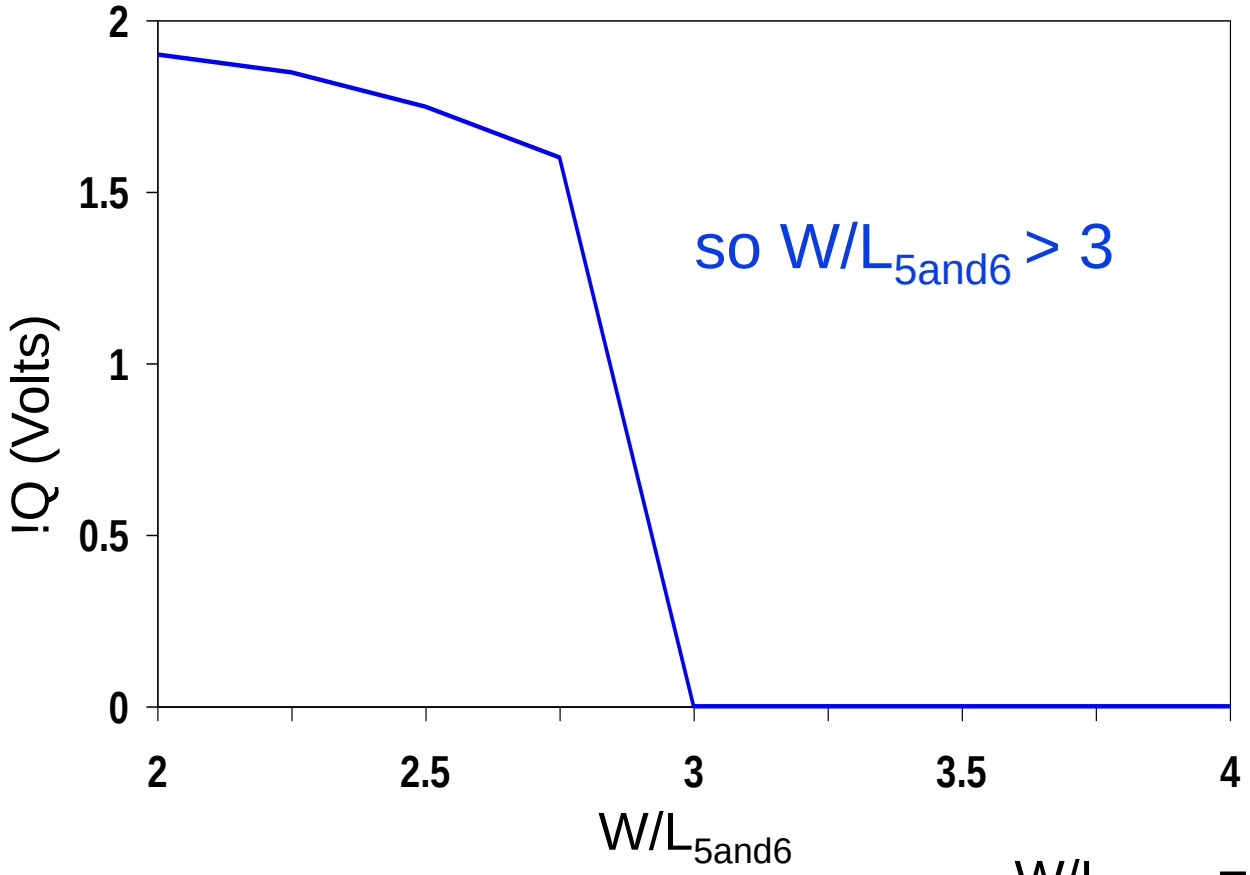


This is not used in datapaths any more, but is a basic building memory cell

Ratioed CMOS Clocked SR Latch



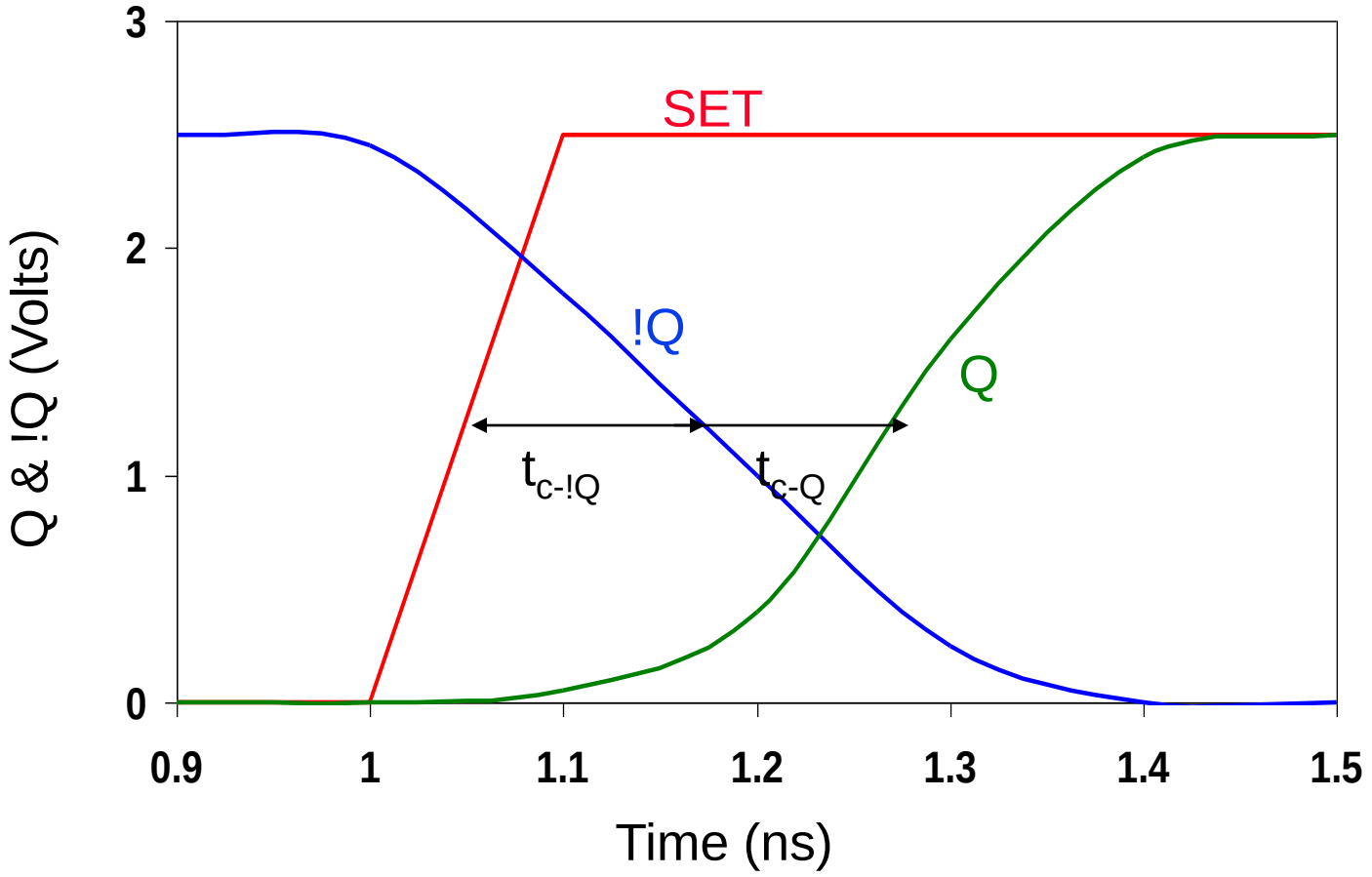
Sizing Issues



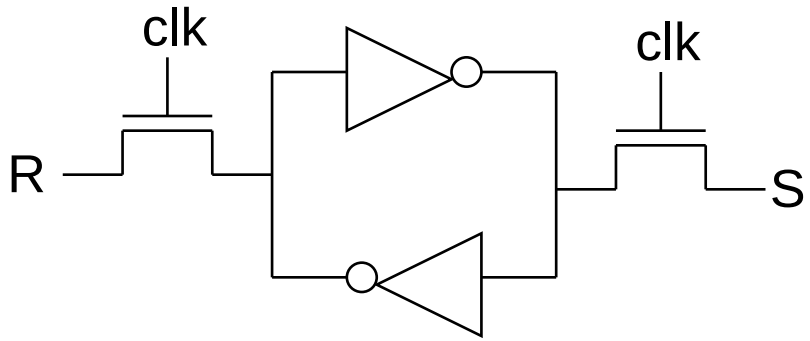
$W/L_{2and4} = 1.5\mu m/0.25\ \mu m$

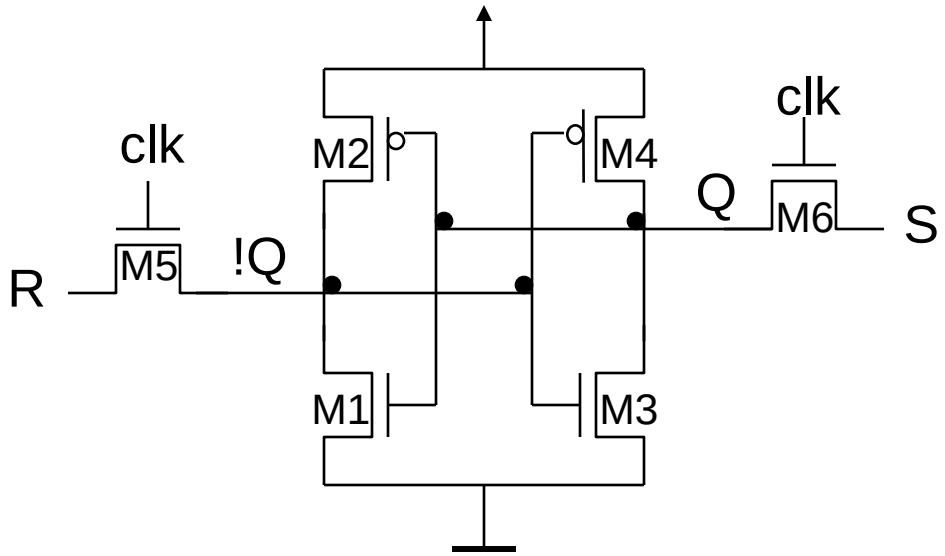
$W/L_{1and3} = 0.5\mu m/0.25\ \mu m$

Transient Response



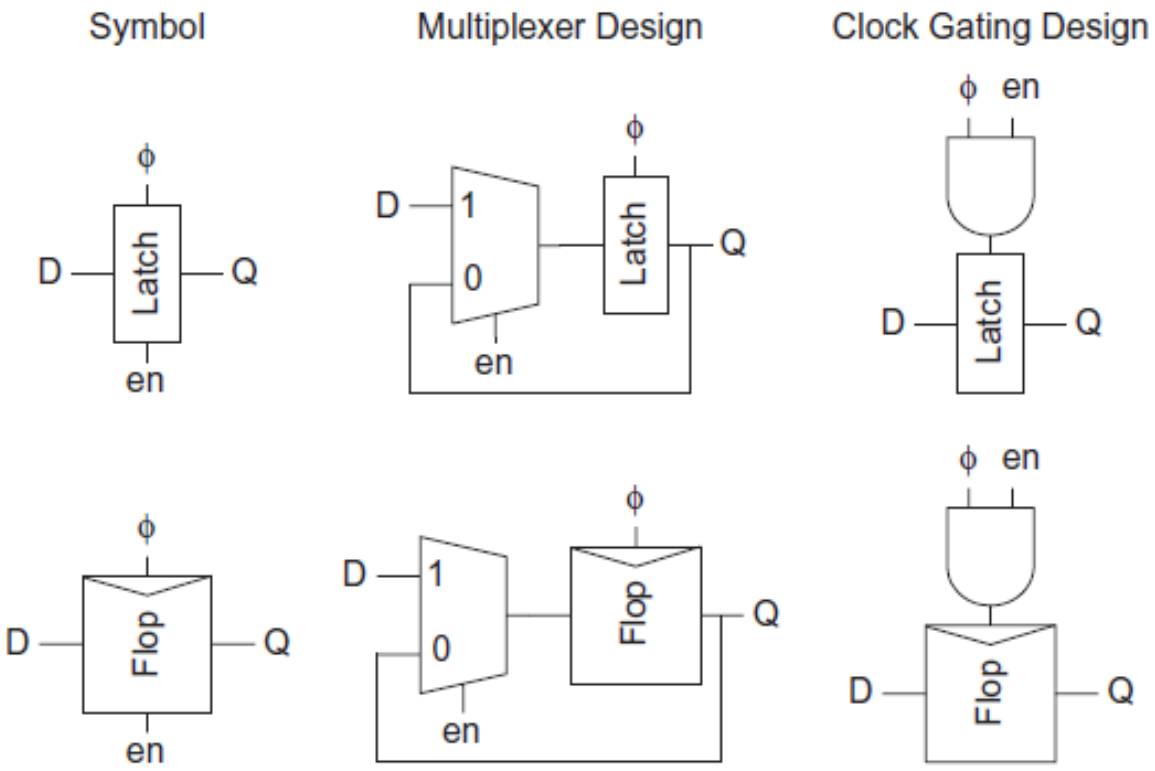
6 Transistor CMOS SR Latch





Enable

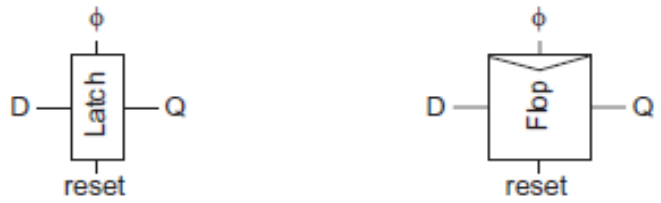
- Enable: ignore clock when en = 0
  - Mux: increase latch D-Q delay
  - Clock Gating: increase en setup time, skew



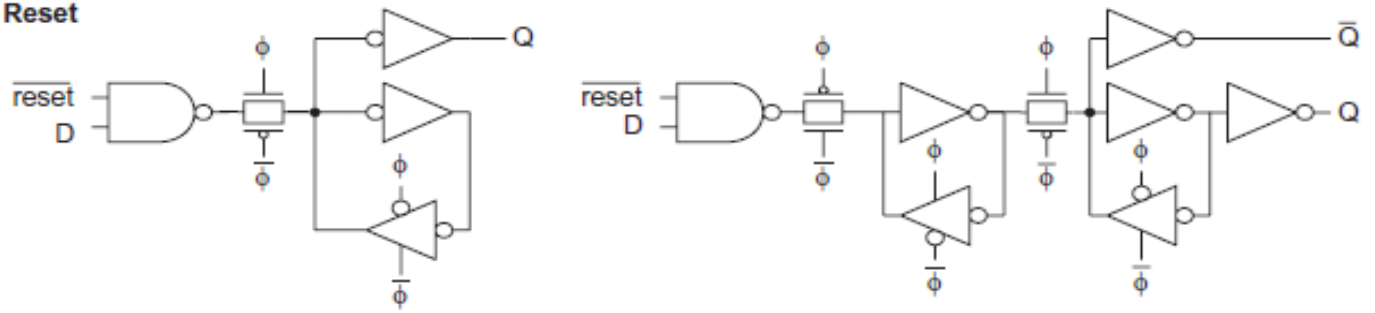
Reset

- Force output low when reset asserted
- Synchronous vs. asynchronous

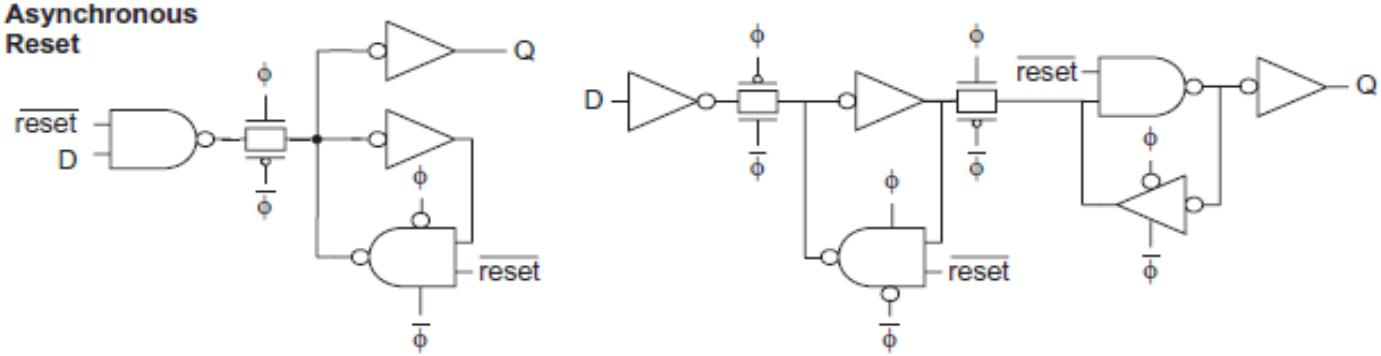
Symbol



Synchronous Reset

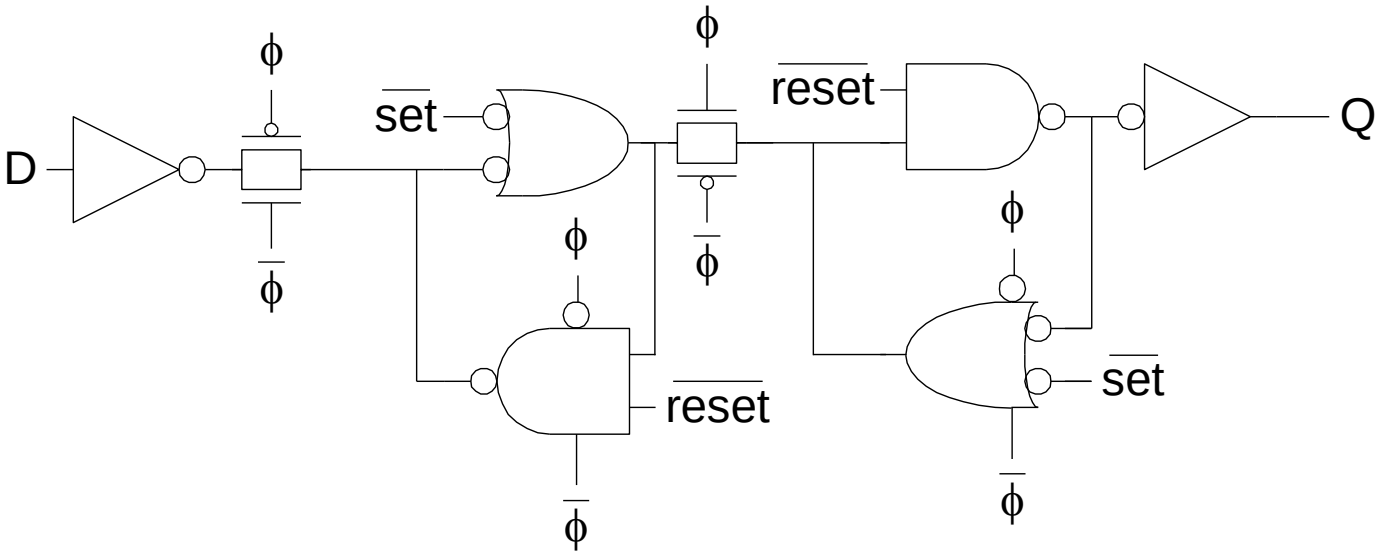


Asynchronous Reset



Set / Reset

- Set forces output high when enabled
- Flip-flop with asynchronous set and reset



جلسه آینده

- درس بعدی
  - مدار های ترتیبی پویا